ALPHA & OMEGA SEMICONDUCTOR

AOZ32063MQV

5V to 60V, Three-Phase Motor Driver

General Description

The AOZ32063MQV is a high performance three- phase brushless, DC motor driver. It is able to drive three half-bridges consisting of six N-channel power MOSFETs up to 60V for three-phase application.

The AOZ32063MQV uses a bootstrap capacitor to generate a supply voltage for the high-side MOSFET driver. The internal trickle-charge circuit maintains a sufficient gate driver voltage at 100% duty cycle. The device features multiple protection functions such as internal safety features including shoot-through protection, adjustable dead-time control, under-voltage lockout, over current protection and over temperature protection, and has a reporting mechanism.

The AOZ32063MQV is available in a 4mm×4mm QFN-28L package and is rated over a -40°C to +125°C ambient temperature range.

Features

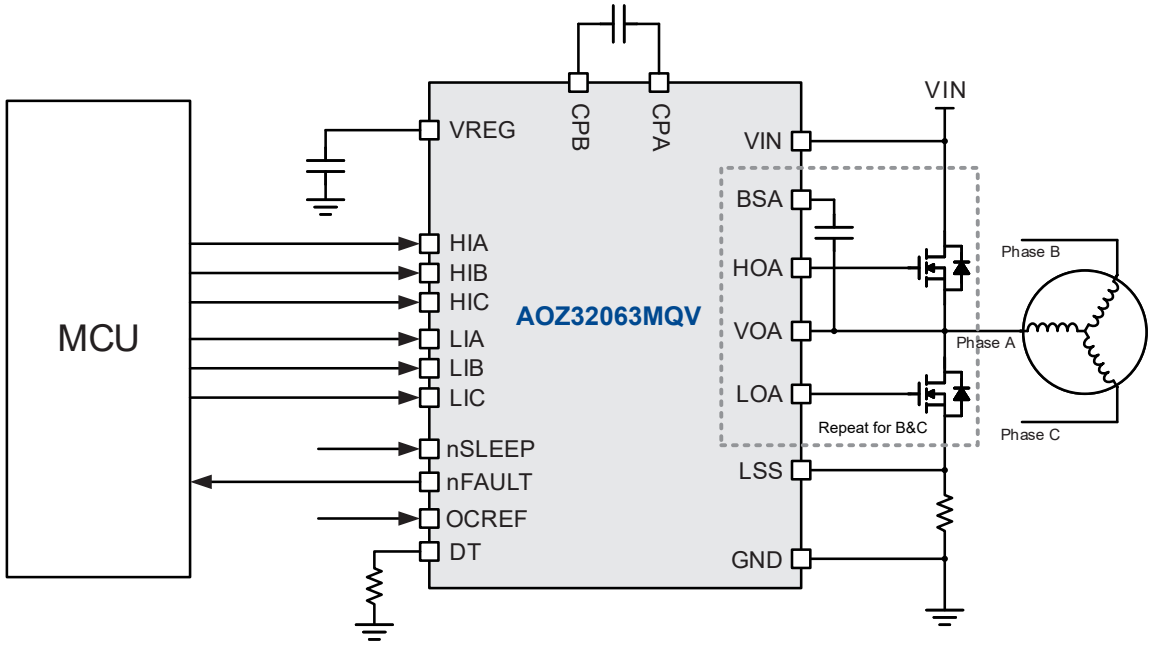
- Wide 5V to 60V input voltage range
- Integrated bootstrap diode and 70V V_{BST} maximum voltage
- Bootstrap Gate Driver with Trickle-Charge Circuit Supports 100% Duty Cycle Operation
- Adjustable dead-time control to prevent shoot-through
- Sleep mode for power saving of battery powered application
- Short circuit protection
- Over current protection
- Thermal shutdown and UVLO protection
- Fault indication output

Applications

- Three-Phase, Brushless, DC Motors
- Permanent Magnet Synchronous Motors
- Fans and pumps
- Power tools
- E-bikes

GREEN Product

Typical Application

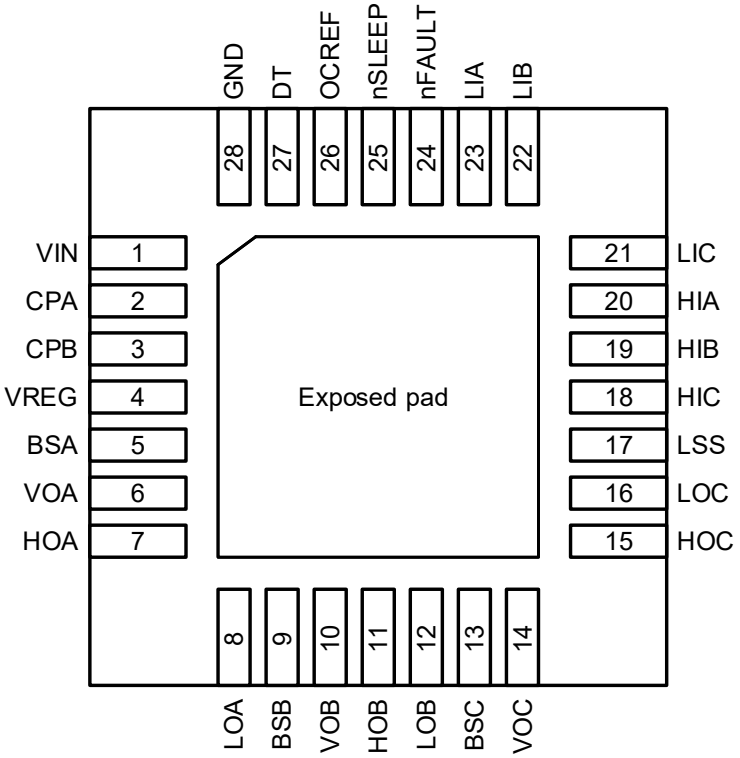


Ordering Information

Part Number	Ambient Temperature Range	Package	Environmental
AOZ32063MQV	-40 °C to +125 °C	QFN4x4-28L	Green

AOS products are offered in packages with Pb-free plating and compliant to RoHS standards.
Please visit https://aosmd.com/sites/default/files/media/AOSGreenPolicy.pdf for additional information.

Pin Configuration



QFN4x4-28L
(Top Transparent View)

Pin Description

Pin Number	Pin Name	Pin Function
1	VIN	Input supply voltage.
2	CPA	Internal charging pump. Connect a ceramic capacitor between CPA and CPB.
3	CPB	
4	VREG	Gate driver power supply output. Connect a ceramic capacitor between VREG and ground.
5	BSA	Bootstrap output, phase A. Connect a ceramic capacitor between BSA and VOA for supplying high-side MOSFET.
6	VOA	High-side source connection phase A.
7	HOA	High-side gate driver output, phase A.
8	LOA	Low-side gate driver output, phase A.
9	BSB	Bootstrap output, phase B. Connect a ceramic capacitor between BSB and VOB for supplying high-side MOSFET.
10	VOB	High-side source connection phase B.
11	HOB	High-side gate driver output, phase B.
12	LOB	Low-side gate driver output, phase B.
13	BSC	Bootstrap output, phase C. Connect a ceramic capacitor between BSC and VOC for supplying high-side MOSFET.
14	VOC	High-side source connection phase C.
15	HOC	High-side gate driver output, phase C.
16	LOC	Low-side gate driver output, phase C.
17	LSS	Connect to the source of all low-side MOSFETs.
18	HIC	High-side gate driver input, phase C.
19	HIB	High-side gate driver input, phase B.
20	HIA	High-side gate driver input, phase A.
21	LIC	Low-side gate driver input, phase C.
22	LIB	Low-side gate driver input, phase B.
23	LIA	Low-side gate driver input, phase A.
24	nFAULT	Fault indication. Logic low when in a fault state. nFAULT is an Open-drain output.
25	nSLEEP	Sleep mode set pin. Logic low to enter sleep mode, logic high to enable. Internal pull down resistor.
26	OCREF	Reference voltage input for over current protection.
27	DT	Dead-time set pin. Connect a resistor between DT and ground to set the Gate drive dead time.
28	GND	Ground.

Absolute Maximum Ratings

Exceeding the Absolute Maximum ratings may damage the device.

Parameter	Rating
VIN	-0.3V to 65V
CPA	-0.3V to 60V
CPB	-0.3V to 12.5V
VREG	-0.3V to 13V
BSA/B/C	-0.3V to 70V
VOA/B/C	-0.3V to 65V
VOA/B/C(transient, 2µs)	-8V to 65V
HOA/B/C	-0.3V to 70V
HOA/B/C(transient, 2µs)	-8V to 70V
LOA/B/C	-0.3V to 13V
LSS	-0.3V to 4V
All other pins to GND	-0.3V to 6.5V
Junction Temperature(TJ)	+150°C
Storage Temperature(TS)	-65°C to + 150°C
ESD Rating	2KV

Recommended Operating Conditions

The device is not guaranteed to operate beyond the Maximum Recommended Operating Conditions.

Parameter	Rating
Supply Voltage (VIN)	+5V to 60V
OCREF Voltage (V_{OCREF})	0.125V to 2.4V
Ambient Temperature (T_A)	-40°C to +125°C
Package Thermal Resistance (Θ_{JA}) (Θ_{JC})	 50 °C/W 6.3 °C/W

Electrical Characteristics

T_A = 25 °C, VIN = 24 V, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Power Supply						
V_{IN}	Input supply voltage		5		60	V
I_Q	Quiescent current	nSLEEP = 1, gate not switching		1.8	2.3	mA
I_{SLEEP}		nSLEEP = 0			1	µA
VREG						
V_{REG}	VREG output voltage	VIN = 5.5V - 60V	10	11.5	13	V
		VIN = 5V	9			V
f_{CP}	Charge pump frequency			100		kHz
Logic input (HIx, LIx, nSLEEP)						
V_{IL}	Input Logic low Voltage Threshold				0.8	V
V_{IH}	Input Logic high Voltage Threshold		2			V
I_{IL}	Input Logic low bias current	V_{IL} = 0.8V	-20		20	µA
I_{IH}	Input Logic high bias current	V_{IH} = 5V	-20		20	µA
$I_{SLEEP-PD}$	nSLEEP pull-down current			1		uA
R_{PD}	Internal pull-down resistance			600		kΩ

Electrical Characteristics

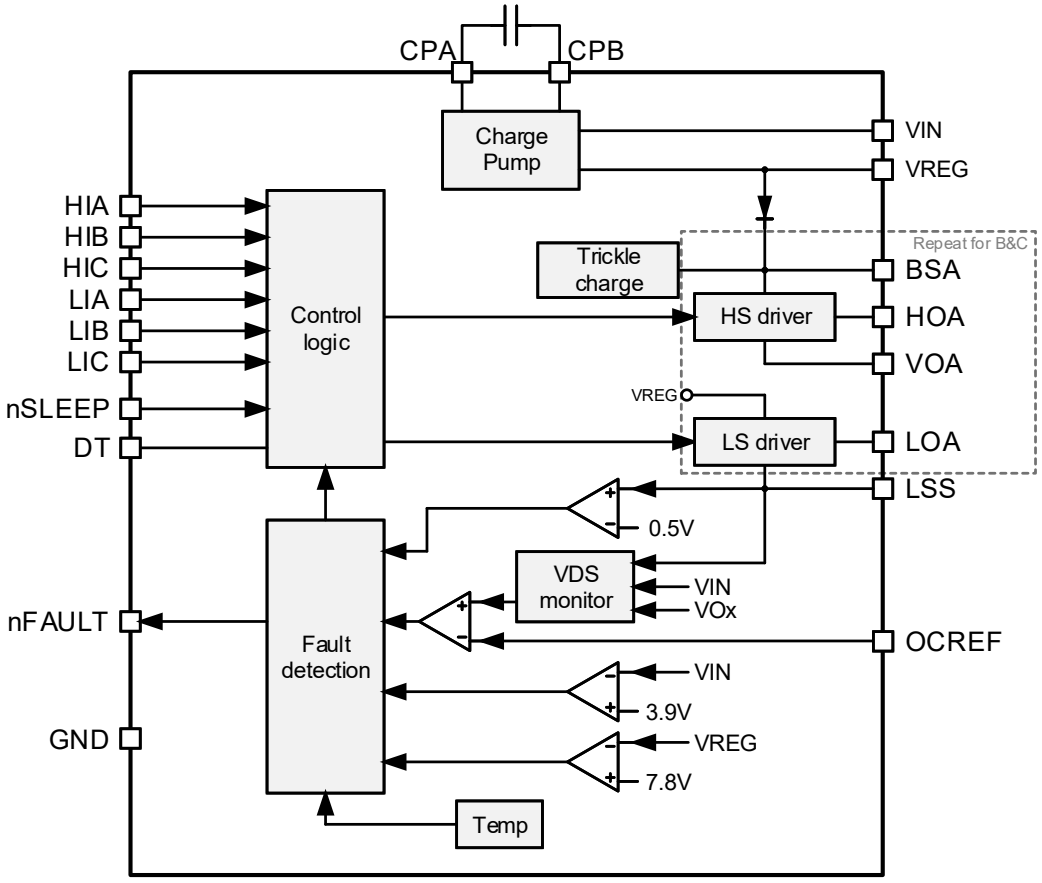
T_A = 25 °C, VIN = 24 V, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Fault Output (Open-Drain Output)						
V_{OL}	Output low voltage	I_O = 5mA			100	mV
I_{OH}	Output high leakage current	V_O = 3.3V			1	µA
Gate Driver						
V_{F_BOOT}	Bootstrap diode forward voltage	VIN = V_{REG} = 12V, LIx = High, I_D= 10mA			0.1	V
		VIN = V_{REG} = 12V, LIx = High, I_D= 100mA			1	V
I_{SOURCE} (1)	Maximum source current			0.8		A
I_{SINK} (1)	High side maximum sink current			1		A
	Low side maximum sink current			2		A
R_{UP}	Gate drive pull-up resistance	V_{DS} = 1V		8		Ω
R_{HS-DN}	HS gate drive pull-down resistance	V_{DS} = 1V	1		5.5	Ω
R_{LS-DN}	LS gate drive pull-down resistance	V_{DS} = 1V	1		5.8	Ω
R_{LS-PDN}	LS passive pull-down resistance			590		kΩ
t_{LS}	LS automatic turn-on time	At power-up		0.5		µs
t_{DEAD}	Dead time	R_{DT} = 100kΩ		5		µs
		R_{DT} = 10kΩ		0.7		µs
		DT tied to GND		150		ns
Protection Circuits						
V_{INRISE}	UVLO rising threshold		3.3	3.9	4.5	V
V_{INHYS}	UVLO hysteresis			800		mV
$V_{REG\ RISE}$	VREG rising threshold		6.8	7.8	8.5	V
$V_{REG\ HYS}$	VREG hysteresis			0.6	1	V
t_{REG}	VREG start-up delay			850		µs
V_{OCREF}	OC_REF threshold	V_{OC} = 1V	0.8	1	1.2	V
		V_{OC} = 2.4V	2.18	2.4	2.62	V
t_{OCd}	OCP deglitch time			3		µs
$V_{LSS-OCP}$	LSS OCP threshold		0.4	0.5	0.6	V
t_{SLEEP}	SLEEP wake-up time			0.6		ms
T_{OTP}	Thermal shutdown temperature			150		°C

Note:

1. Guarantee by design.

Functional Block Diagram



Detailed Description

The AOZ32063MQV is a three-phase brushless motor driver, can driver for six external N-channel MOSFET. The gate drivers can drive up to 0.8A Source Current and 1A sink current. The AOZ32063MQV operates over a wide input voltage range of 5V to 60V, when the input power is below 12V, the built-in charge pump will boost the gate drive voltage. AOZ32063MQV has a low power sleep mode and provides flexible functions such as setting dead time and setting over-current protection point. The AOZ32063MQV provides several protection features, such as VIN under voltage protection, over-current protection and short-circuit protection, and over temperature protection, which allow the device covers a wide range of applications.

Fault events are indicated by the nFAULT pin.

Charge Pump

The AOZ32063MQV built-in charge pump will boost the gate drive voltage (VREG) to 10 ~ 12V, even if the input power supply voltage drops to 5V. The charge pump must connect a ceramic capacitor between CPA and CPB, its value should be 0.47uF. The capacitor rating must be able to withstand the maximum VIN voltage.

Gate Drive Power Supplies (VREG)

The gate drive voltage depends on the input voltage VIN. When VIN exceeds 12V, the VREG voltage is generated by the LDO; when VIN falls below 12V, the VREG voltage is generated by the charge pump. VREG requires a 10µF bypass capacitor to ground. This should be at least 16V for ceramic capacitors.

Bootstrap Circuit Description

The high-side gate is driven using a bootstrap circuit with integrated diode. The bootstrap diode is integrated and an external bootstrap capacitor is used between the BSx and VOx pins. The device uses a trickle charge pump integrated circuit and can support 100% duty cycle control.

A trickle charge pump is connected to the BSx node to prevent voltage drops due to leakage current from the driver and external MOSFETs.

The low-side gate output is directly driven by VREG.

Sleep Mode

AOZ32063MQV has very low sleep power consumption. When entering sleep mode, most of the circuits are turned off, and the power consumption can be less than 1uA.

Control whether the system enters sleep through nSLEEP pin.

When

- nSLEEP = high is enable, normal operation mode
- nSLEEP = low is sleep mode

When the system wakes up from sleep, after about 0.6ms, the gate driver will start to work.

Furthermore, it is strongly recommended that the nSLEEP signal transitions from 0V to 2V in a time not exceeding 1ms.

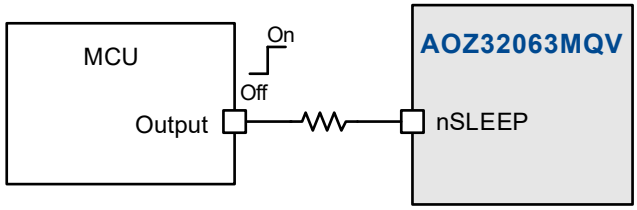


Figure 1. nSLEEP Pin Application Circuit

Control Logic

When nSLEEP is pulled high, HOx and LOx follow their respective HIx and LIx signals through the gate driver to drive MOSFETs, and the internal circuit will also judge whether the HIx/LIx signals are high at the same time to avoid shoot-through of High/Low side MOSFETs.

The truth table of the control logic is as follows:

Table 1. Control Logic Table

HIx	LIx	HOx	LOx	VOx
L	L	L	L	High impedance
H	L	H	L	VIN
L	H	L	H	GND
H	H	L	L	High impedance

Fault Indicator

The nFAULT pin is an open drain output, which is connected with a pull high resistor to report faults. Users can use this signal to judge whether the AOZ32063MQV is in a normal or faulty state. When a fault occurs, nFAULT pin is pull low.

The following is the protection mechanism that the fault pin will report.

- VIN UVLO: When the input voltage VIN drops below VIN_{RISE} UVLO rising threshold.
- VREG UVLO: After power-up, when the voltage on VREG drops below $VREG_{RISE}$ UVLO rising threshold.

- LSS OCP: When the LSS voltage (the voltage across the shunt resistor) exceeds the $V_{LSS-OCP}$ threshold.
- SCP (VDS Sensing): The VDS voltage is generated by the voltage drop across the external MOSFET $R_{DS(ON)}$ connected. When the VDS voltage exceeds the voltage set by the OC_REF threshold, a short circuit is recognized. VDS threshold can be set from 1 V to 2.4 V.
- Over temperature: When the die temperature exceeds the trip point of the thermal shutdown temperature limit (OTP).

When the fault condition is to be cleared, the device can be re-enabled by issuing a reset pulse to the nSLEEP pin.

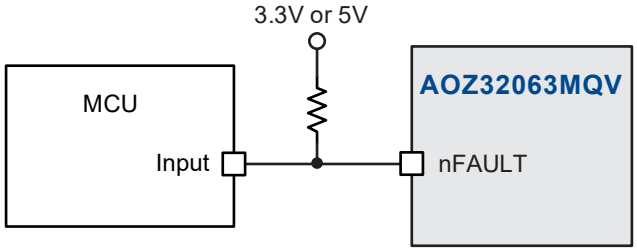


Figure 2. nFAULT Pin Application Circuit

Dead Time and Shoot-Through Prevention

AOZ32063MQV has a built-in dead time adjustment function. The dead time can be adjusted only by adjusting the resistance value of the DT pin to ground. Users can set different dead time for different application conditions.

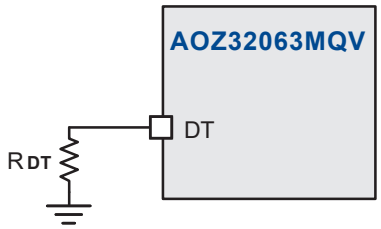


Figure 3. Dead Time Resistor

Table 2. Dead Time (DT Pin) Setting Table

DT pin	Dead time(μs)
Open	5.35
Tied to GND	0.15
Add R	Calculated by the following formula t_{dead} (us)=0.052×R_{DT} (KΩ)+0.15

The High side and Low side are independently controlled by individual signals. In order to prevent the high side and low side MOSFETs from being turned on at the same time, AOZ32063MQV has a built-in shoot-through prevention mechanism. The following figure illustrates the dead time and shoot-through prevention mechanism.

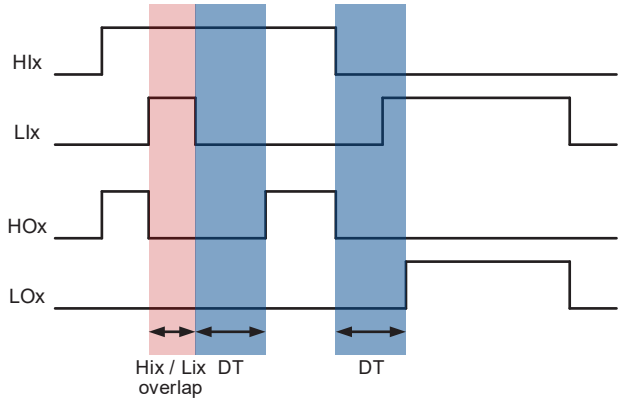


Figure 4. Dead Time and Shoot-Through Prevention

Over Current Protection (LSS OCP)

When the low-side MOSFET is turned on, the total system current flows through the shunt resistor between LSS and GND, and the voltage difference generated by the shunt resistor is the voltage of LSS.

When this voltage exceeds $V_{LSS-OCP}$ 0.5v, it will be judged as over-current and protected. For example, if a 100mΩ resistor is used, a 5A current will result in a 500mV drop, activating the over-current protection.

After detecting over-current event, all gate driver outputs are driven low to disable the external MOSFETs and the nFAULT pin is drive to low.

If the OCP function isn't desired, both LSS and MOSFET source terminals should be connected to ground. The other way to disable OCP is connection a 100KΩ resistor form VREG to OCREF pin or making the OCREF pin floating.

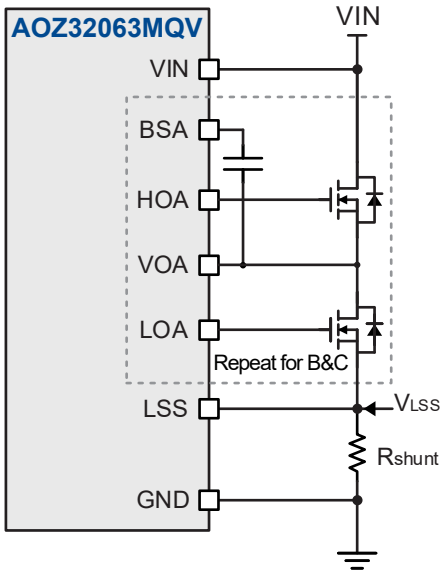


Figure 5. LSS Voltage (V_{LSS})

Short Circuit Protection (MOSFET VDS Sensing)

AOZ32063MQV has an adjustable VDS voltage monitor for detecting external power MOSFET over-current or short-circuit conditions. The OC_REF voltage is usually supplied externally from a convenient supply resistor divider. When the VDS voltage exceeds the voltage set by the OC_REF threshold, a short circuit is recognized. VDS threshold can be set from 1 V to 2.4 V.

After detecting short-circuit event, all gate driver outputs are driven low to disable the external MOSFETs and the nFAULT pin is drive to low. This protection function can be disabled by connection a 100KΩ resistor from VREG to OCREF pin or making the OCREF pin floating.

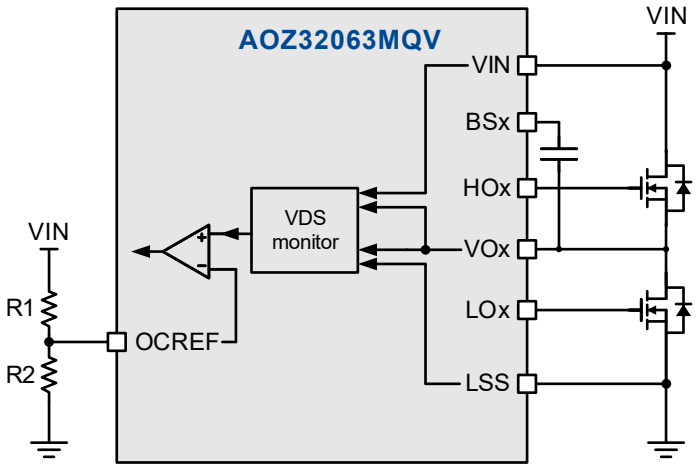


Figure 6. MOSFET VDS Sensing and OCREF Pin Application Circuit

Over Temperature Protection (OTP)

When the system is working, if the temperature of the die is too high and exceeds the internally set temperature protection level (about 150°C), AOZ32063MQV automatically enters the over-temperature protection, the gate driver stops working and does not output signals, and the nFAULT pin is pull low at the same time to maintain the latched state. Until reset by nSLEEP or VIN UVLO.

Layout Guidelines

A good layout is very important for noise suppression and driver performance.
List the following five-point layout suggestions and refer to the figure below:

1. Input capacitors C1&C2 should be connected to the VIN pins and the GND pins as close as possible to reduce the switching spikes. It is recommended to use ceramic capacitors above 10μF and 0.1μF to match.
2. The capacitor C3 of the charge pump pin should be very close to the IC.
3. The voltage stabilizing capacitor C4 should be placed as close as possible to the VREG pin to effectively reduce noise.
4. The bootstrap capacitor needs to be close to the corresponding pin.
5. The dead time resistor R_DT should be close to the DT pin.

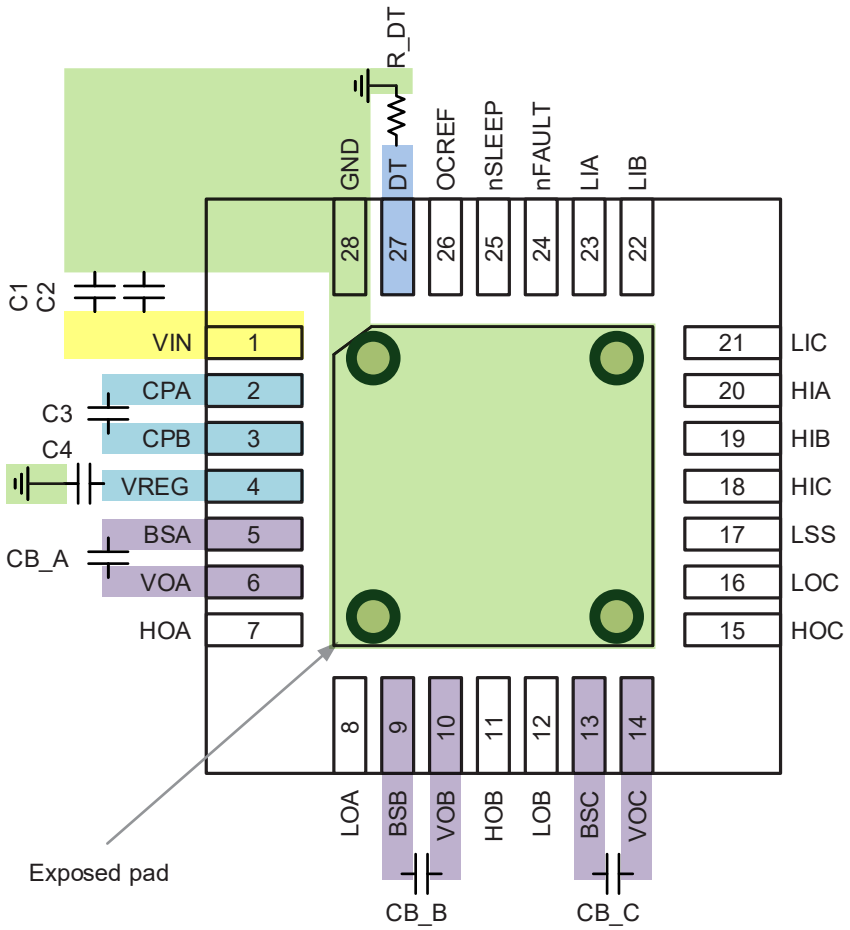
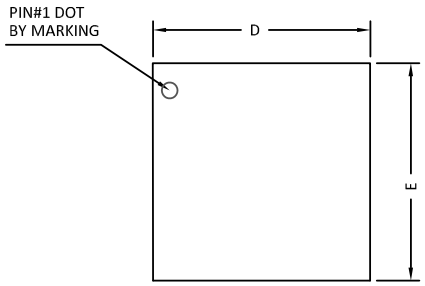
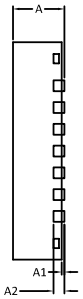


Figure 7. Layout Reference Diagram

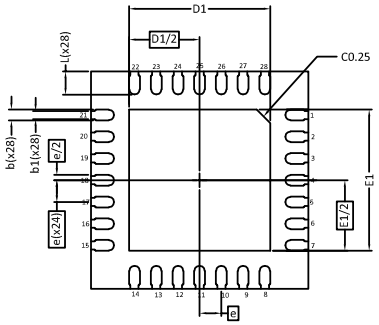
Package Dimensions, QFN4x4-28L



TOP VIEW

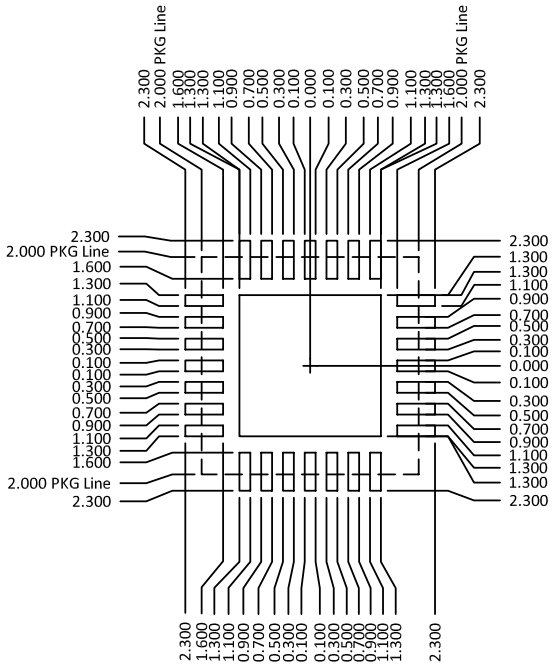


SIDE VIEW



BOTTOM VIEW

RECOMMENDED LAND PATTERN



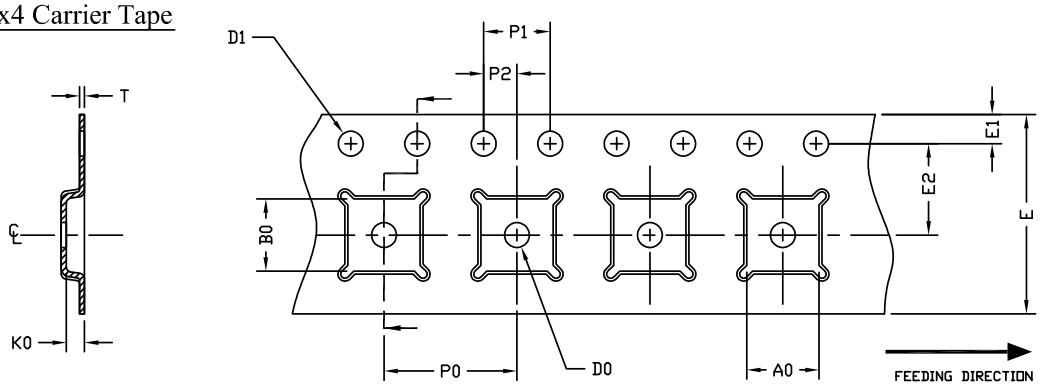
SYMBOLS	DIMENSION IN MM			DIMENSION IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.85	0.90	0.95	0.033	0.035	0.037
A1	0.00	---	0.05	0.000	----	0.002
A2	0.15	0.20	0.25	0.006	0.008	0.010
b	0.15	0.20	0.25	0.006	0.008	0.010
b1		0.150 REF			0.007 REF	
D	3.90	4.00	4.10	0.154	0.157	0.161
D1	2.50	2.60	2.70	0.098	0.102	0.106
E	3.90	4.00	4.10	0.154	0.157	0.161
E1	2.50	2.60	2.70	0.098	0.102	0.106
e		0.40BSC			0.020BSC	
L	0.35	0.40	0.45	0.014	0.016	0.018

UNIT: mm

NOTE:
1. CONTROLLING DIMENSION IS MILLIMETER.
CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.

Tape and Reel Dimensions, QFN4x4-28L

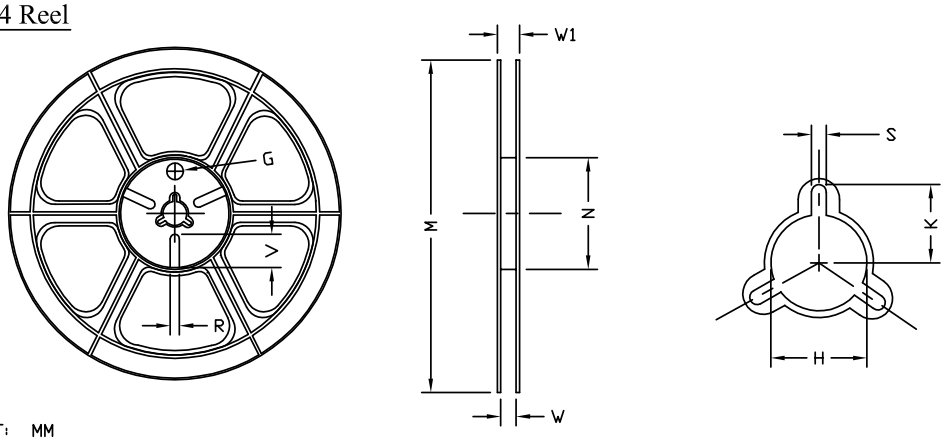
QFN4x4 Carrier Tape



UNIT: MM

PACKAGE	A0	B0	K0	D0	D1	E	E1	E2	P0	P1	P2	T
QFN4x4 (12 mm)	4.35 ±0.10	4.35 ±0.10	1.10 ±0.10	1.50 MIN.	1.50 +0.1 −0.0	12.0 ±0.3	1.75 ±0.10	5.50 ±0.05	8.00 ±0.10	4.00 ±0.10	2.00 ±0.05	0.30 ±0.05

QFN4x4 Reel



UNIT: MM

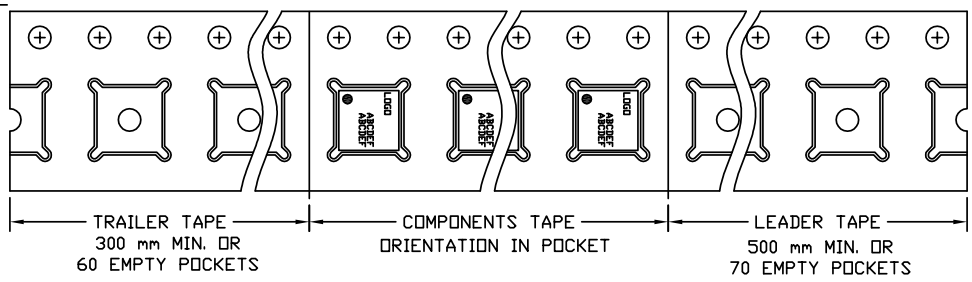
TAPE SIZE	REEL SIZE	M	N	W	W1	H	K	S	G	R	V
12 mm	ø330	ø330.0 ±2.0	ø79.0 ±1.0	12.4 +2.0 −0.0	17.0 +2.6 −1.2	ø13.0 ±0.5	10.5 ±0.2	2.0 ±0.5	---	---	---

QFN4x4 Tape

Leader / Trailer & Orientation

Normal

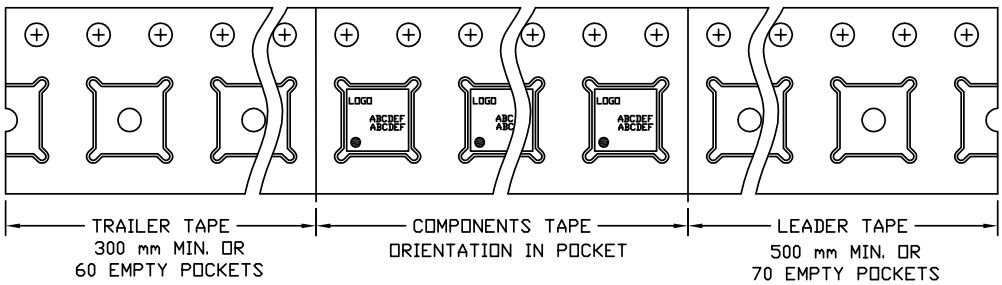
Unit Per Reel: 3000pcs



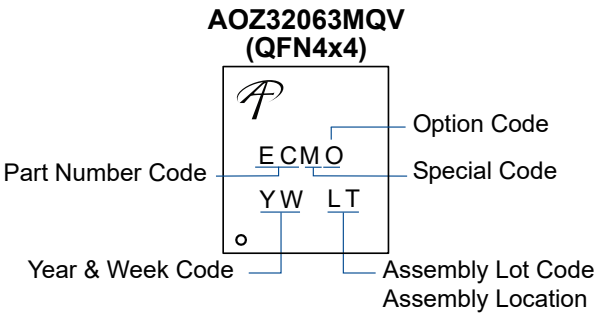
Leader / Trailer & Orientation

Special

Unit Per Reel: 3000pcs



Part Marking



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2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.